LOW DROP-OUT VOLTAGE REGULATOR AND AN ADAPTIVE FREQUENCY COMPENSATION METHOD FOR THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a voltage regulator circuit, and more particularly to a low drop-out voltage regulator and an adaptive frequency compensation method for the same.

Description of the Related Art

[0002] Voltage regulators with a low drop-out (LDO) are commonly used in the power management systems of PC motherboards, notebook computers, mobile phones, and many other products. Power management systems use LDO voltage regulators as local power supplies, where a clean output and a fast transient response are required. LDO voltage regulators enable power management systems to efficiently supply additional voltage levels that are smaller than the main supply voltage. For example, the 5V power systems of many PC motherboards use LDO voltage regulators to supply local chipsets with a clean 3.3V signal.

[0003] Although LDO voltage regulators do not convert power very efficiently, they are inexpensive, small, and generate very little frequency interference. Furthermore, LDO voltage regulators can provide a local circuit with a clean voltage that is unaffected by current fluctuations from other areas of the power system. LDO voltage regulators are widely used to supply power to local circuits when the power

consumption of the local circuit is negligible with respect to the overall load of a power system.

[0004] An ideal LDO voltage regulator should provide a precise DC output, while responding quickly to load changes and input transients. Due to the nature of its use in mass-produced products such as computers and mobile phones, LDO voltage regulators should also have a simple design and a low production cost.

[0005] A typical LDO voltage regulator consists of a feedback-control loop coupled to a pass element. The feedback-control loop modulates the gate voltage of the pass element to control its impedance. Depending on the gate voltage, the pass element supplies different levels of current to an output section of the power supply. The modulation of the gate voltage is done in a manner such that the LDO voltage regulator outputs a steady DC voltage, regardless of load conditions and input transients.

[0006] One problem with traditional LDO circuits is that they are prone to instability. The output section of a traditional LDO circuit includes an output capacitor coupled to the load. This coupling introduces a dominant pole into the feedback circuit. Traditional LDO circuits rely on the equivalent series resistance (ESR) of the output capacitor to restore stability. Within a narrow range of values, the ESR can compensate for the output pole by introducing a zero into the LDO voltage regulator feedback-control loop. Within a range of operating conditions, the zero can increase the phase margin of the LDO voltage regulator.

[0007] Unfortunately, the ESR is a parasitic component of the output capacitor and its value cannot easily be determined or controlled to a high precision. The ESR of a capacitor changes significantly with respect to load, temperature, and possibly other factors. If the ESR increases or decreases too much, then the ESR zero will no longer

compensate for the pole introduced by the output capacitor.

[0008] Another problem with traditional LDO voltage regulators is that the ESR adversely affects the transient response of the LDO voltage regulator. For a LDO voltage regulator to respond rapidly to transients, the ESR must be reduced as much as possible. However, a small ESR will shift the compensating zero of the ESR to a higher frequency, where it will no longer compensate for the pole induced by the output capacitor. In a traditional LDO voltage regulator, the ESR cannot be reduced without threatening the stability of the entire circuit.

[0009] Another problem with traditional LDO voltage regulators is that they have a slow transient response under light loads. Under light loads, the frequency of the output capacitor pole decreases. However, the frequency of the stabilizing zero does not change, and the cross-over frequency of the LDO voltage regulator is reduced. Traditional LDO voltage regulators are not designed to enable the stabilizing zero to follow the output pole. If the position of the zero could also be shifted to a lower frequency, the cross-over frequency of the LDO voltage regulator would not be reduced under light loads.

[0010] Traditional LDO voltage regulators are prone to instability since the ESR cannot be controlled precisely. Furthermore, their performance suffers degradation under light load conditions. Therefore, there is a need for an improved low drop-out voltage regulator that is suitable for a wider range of capacitive loads while eliminating the minimum ESR restriction of the output capacitor.

SUMMARY OF THE INVENTION

[0011] An objective of the present invention is to provide a low drop-out (LDO)

voltage regulator that can provide DC-DC conversion with very tight output control for computer motherboards, notebook computers, mobile phones, and other products.

[0012] Another objective of the present invention is to provide an adaptive frequency compensation scheme for a LDO voltage regulator, such that the LDO voltage regulator is stable under a wide range of load conditions.

[0013] Another objective of the present invention is to provide a LDO voltage regulator with generally improved transient response.

[0014] Another objective of the present invention is to provide a LDO voltage regulator with a faster transient response under light-load conditions.

[0015] According to one aspect of the present invention, to improve stability, the adaptive frequency compensation scheme generates an equivalent series resistance (ESR). This introduces a zero into the feedback loop. The frequency of the generated zero can be controlled precisely. According to the present invention, it is possible to ensure circuit stability without controlling the lower limit of the equivalent series resistance (ESR) of the output capacitor. This is preferable, because the ESR of a capacitor can vary unpredictably with respect to temperature and load. Furthermore, the resistance of the current-controlled resistor can be varied in response to the output current, so that the frequency of the zero will follow the frequency of the output pole. This can help improve the transient response of the circuit.

[0016] According to another aspect of the present invention, for a DC output during transient-state operation, the output ESR should be low, and the cross-over frequency of the LDO voltage regulator should be high. The adaptive frequency compensation scheme of the present invention ensures the stability of the LDO voltage regulator with a generated ESR, rather than the ESR of the output capacitance. There is

no need to control the lower limit of the ESR of the output capacitance. According to the present invention, the output section can contain an arbitrarily low capacitive ESR without endangering system stability. In practice, this enables the LDO voltage regulator to be optimized for improved transient performance.

[0018] Still further objects and advantages will become apparent from a consideration of the ensuing description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0020] FIG. **1** shows a prior-art LDO voltage regulator.

[0021] FIG. **2** shows a LDO voltage regulator according to the present invention.

[0022] FIG. **3** shows an embodiment of a current-controlled resistor according to the present invention.

[0023] FIG. **4** shows an embodiment of a current-controlled current sink according to the present invention.

[0024] FIG. **5** shows an embodiment of building a large resistance of the present invention.

[0025] FIG. **6** is a graph showing the approximate range of ESR values that guarantee the stability of the prior-art LDO voltage regulator.

[0026] FIG. **7A** shows the transient response of the prior-art LDO voltage

regulator.

[0027] FIG. **7B** shows the transient response of the LDO voltage regulator according to the present invention.

[0028] FIG. **8A** compares the pole-zero locations and cross-over frequencies of the transfer function of the prior-art LDO voltage regulator. The solid line indicates the transfer function under a heavy-load and the dotted line indicates the transfer function under a light-load.

[0029] FIG. **8B** compares the pole-zero locations and cross-over frequencies of the transfer function of the LDO voltage regulator according to the present invention. The solid line indicates the transfer function under a heavy-load and the dotted line indicates the transfer function under a light-load.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] Referring now to the drawings wherein the contents are for purposes of illustrating the preferred embodiment of the invention only and not for purposes of limiting same, FIG. **1** shows a basic configuration of a prior-art low drop-out (LDO) voltage regulator.

[0031] The prior-art LDO voltage regulator includes an unregulated DC input port $\mathbf{V_{IN}}$, an output pass transistor **10**, a regulated DC output port $\mathbf{V_{OUT}}$, and an output section comprising a load resistance **20**, an output capacitor **21** and a parasitic equivalent series resistance (ESR) **22**. The prior-art LDO voltage regulator further comprises a voltage divider having a voltage divider terminal $\mathbf{V_{FB}}$, and two resistors **31** and **32**. The prior-art LDO voltage regulator further comprises a feedback-control circuit. The feedback-control circuit comprises an error amplifier **40**, a reference voltage

port V_{REF}. The output impedance of the error amplifier **40** is represented as a resistor **41**, which is connected from an output of the error amplifier **40** to the ground reference. A gate of the output pass transistor **10** has a parasitic capacitance represented as a capacitor **42**, which is connected from the gate of the output pass transistor **10** to the ground reference.

[0032] The unregulated DC input port V_{IN} is connected to a source of the output pass transistor **10**. A drain of the output pass transistor **10** is connected to the regulated DC output port V_{OUT}. The load resistance **20** and the output capacitor **21** are connected in parallel between the regulated DC output port V_{OUT} and the ground reference. The output capacitor **21** includes a parasitic ESR **22**.

[0033] The regulated DC output port V_{OUT} is connected to the feedback-control circuit via the voltage divider. The resistors **31** and **32** are connected in series between the regulated DC output port V_{OUT} and the ground reference. The voltage divider terminal V_{FB} is in between the resistors **31** and **32**. The voltage divider terminal V_{FB} is connected back to a positive input of the error amplifier **40**. The reference voltage port V_{REF} is connected to a negative input of the error amplifier **40**. An output of the error amplifier **40** is connected to the gate of the output pass transistor **10**. Operation of this circuit will be well known to those skilled in the art.

[0034] As discussed, the prior-art circuit is prone to instability. If the slope at the cross-over frequency becomes less than –40 dB per decade, the system will be unstable. The stability of the circuit depends on the zero introduced by the parasitic ESR **22** of the output capacitor **21**. However, the magnitude of the parasitic resistance can vary greatly with respect to small changes in the operating conditions of the circuit (load, temperature, etc). This can change the position of the zero, and cause the circuit

to become unstable. FIG. **6** shows the range of values for the ESR that guarantee stability, for a typical prior-art LDO voltage regulator. It is important to notice that this range changes significantly with respect to the load current.

[0035] Even if a stable ESR could be provided, it would adversely affect the transient performance of the circuit. FIG. **7A** illustrates the effect of the ESR on the transient response of the prior-art LDO voltage regulator. During load changes, a high ESR will result in a less precise DC output. The higher the output ESR is, the deviation ΔV from the output voltage will be increased.

[0036] FIG. **2** illustrates the basic scheme of a LDO voltage regulator circuit **300** according to the present invention. Details of the reference voltage supply circuit (which may be entirely conventional) have been omitted for simplicity. Like reference numerals are used where components correspond to those of the prior art arrangements described above. It will be seen that the illustrated circuit may be regarded as conventional in so far as it comprises an error amplifier **40** supplying a gate voltage to a gate signal terminal V_{GATE}. The gate signal terminal V_{GATE} controls a gate of a P-MOSFET based output pass transistor **10**. A reference voltage V_{REF1} is supplied to a negative input of the error amplifier **40**. When turned on, the output pass transistor **10** supplies power from an unregulated DC input port V_{IN} to a regulated DC output port V_{OUT}. A load resistance **20** and an output capacitor **21** having a parasitic ESR **22** are connected in parallel from the regulated DC output port V_{OUT} to the ground reference.

[0037] The feedback-control circuit of the present LDO voltage regulator is substantially different from that of prior-art LDO voltage regulators. To supply a feedback signal to the error amplifier **40**, the feedback-control circuit according to the present invention includes an AC feedback terminal V_{FBAC} and a DC feedback terminal

V_{FBDC}. A source of a transistor **45** is connected to the unregulated DC input port V_{IN}. A gate of the transistor **45** is connected to the gate signal terminal V_{GATE}. A drain of the transistor **45** is connected to the AC feedback terminal V_{FBAC}. The AC feedback terminal V_{FBAC} is connected to a positive input of the error amplifier **40** via a capacitor **43**. The DC feedback terminal V_{FBDC} is connected from the regulated DC output port V_{OUT} to the positive input of the error amplifier **40** via a resistor **44**. The DC feedback terminal V_{FBDC} is equivalent to the regulated DC output port V_{OUT}.

[0038] The LDO voltage regulator according to the present invention further differs from prior-art LDO voltage regulators, in that in place of relying upon the parasitic ESR **22** to provide a zero, the circuit includes a current-controlled resistor **100**. The current-controlled resistor **100** is connected between the regulated DC output port V_{OUT} and the AC feedback terminal V_{FBAC}. This introduces a stabilizing zero into the transfer function that depends on the resistance of the current-controlled resistor **100**, instead of depending on the parasitic ESR **22**, as in prior-arts. Because the resistance of the current-controlled resistor **100** can be precisely controlled, it is no longer necessary to depend on the parasitic ESR **22** for the stability of the transfer function.

[0039] Prior-art LDO voltage regulators generally require a minimum value for the ESR of the output capacitor **21**. This stabilizes the circuit, but it also adversely affects the transient response (FIG. **7A**). During load changes, a high ESR will result in a larger deviation from the steady-state DC output voltage. In the LDO voltage regulator according to the present invention, the parasitic ESR **22** can be reduced arbitrarily without endangering system stability. Because of this, it is possible to improve the transient response of the LDO voltage regulator by using a capacitor with a very low ESR for the output capacitor **21**. This allows the LDO voltage regulator to be

optimized for improved transient response, so that the deviation **ΔV** from the output voltage will be reduced (FIG. **7B**).

[0040] The feedback-control circuit of the present invention takes a high-frequency feedback signal from the AC feedback terminal $\mathbf{V_{FBAC}}$. The capacitor **43** is necessary as a DC blocking device, because the AC feedback terminal $\mathbf{V_{FBAC}}$ cannot be used to control the magnitude of the output voltage $\mathbf{V_{OUT}}$. This is because a small current will flow across the current-controlled resistor **100**. This current will change with respect to the magnitude of the output load. As this current changes with respect to output load, the potential drop across the current-controlled resistor **100** will also change.

[0041] Therefore, it is necessary to include a DC feedback terminal $\mathbf{V_{FBDC}}$ to supply the DC component of the feedback signal to the error amplifier **40**. The DC feedback voltage is supplied to the positive input of the error amplifier **40** via the resistor **44**. If the resistance of the resistor **44** is sufficiently large, it will prevent the high-frequency behavior of the LDO voltage regulator from being affected. A typical value for the resistance of the resistor **44** would be about 10 $M\Omega$.

[0042] The transient response of the prior-art LDO voltage regulator deteriorates under light loads. This happens because the frequency of the dominant pole decreases. However, the frequency of the stabilizing zero introduced by the parasitic ESR **22** does not change. This reduces the cross-over frequency, and with that, the transient response of the circuit. FIG. **8A** demonstrates this effect, where the solid-line shows the frequency response under heavy-loads, and the dotted-line indicates the frequency response under light-loads. Because the cross-over frequency decreases from $\mathbf{f_c}$ to $\mathbf{f_c}$' under light-loads, the transient response of the LDO voltage regulator slows down.

When load changes occur, the output of the LDO voltage regulator takes more time **Δt** to adjust (FIG. **7A**).

[0043] To avoid degradation to the transient response under light-load conditions, the resistance of the current-controlled resistor **100** changes with respect to the load. This changes the Bode-plot while maintaining DC stability. FIG. **8B** demonstrates the effect of the current-controlled resistor **100**, where the solid-line shows the frequency response under heavy-loads, and the dotted-line indicates the frequency response under light-loads. Because the cross-over frequency (f_c, f_c') does not change under light-load conditions, the transient response of the LDO voltage regulator does not suffer degradation. FIG. **7B** shows that the time **Δt** required for stabilizing the output voltage of the LDO voltage regulator is substantially shorter than that in the prior-art.

[0044] FIG. **3** shows the current-controlled resistor **100** according to a preferred embodiment of the present invention. The current-controlled resistor **100** consists of three transistors **101, 102** and **103**, a comparator **104**, and a current-controlled current sink **110**. A drain of the transistor **101** is connected to the regulated DC output port V_{OUT}. A gate of the transistor **101** is connected to a gate of the transistor **102** and a drain of the transistor **102**. A source of the transistor **101** is connected to the AC feedback terminal V_{FBAC}. A drain of the transistor **102** is connected to an input current terminal I_1. A source of the transistor **102** is connected to a drain of the transistor **103**. A source of the transistor **103** is connected to a reference voltage terminal V_{REF2}. A gate of the transistor **103** is connected to an output of the comparator **104**. A negative input of the comparator **104** is connected to the AC feedback terminal V_{FBAC}. A positive input of the comparator **104** is connected to the drain of the transistor **103**. An input of the current-

controlled current sink **110** is connected to the input current terminal I_1. An output of the current-controlled current sink **110** is connected to the ground reference.

[0045] The resistance of the current-controlled resistor **100** changes in response to the output current. Therefore, the frequency of the zero generated by the current-controlled resistor **100** can change with respect to the output load. This allows the transient response of the LDO voltage regulator to be optimized under heavy-load and light-load conditions. The operation of this circuit is well known to those skilled in the art, and does not need to be discussed in further detail here.

[0046] FIG. **4** shows the current-controlled current sink **110** according to an preferred embodiment of the present invention. The current-controlled current sink **110** consists of three transistors **111** **112** and **113**. A gate of the transistor **111** is connected to the gate signal terminal V_{GATE}. A source of the transistor **111** is connected to the unregulated DC input port V_{IN}. A drain of the transistor **111** is connected to a drain of the transistor **113**, a gate of the transistor **113**, and a gate of the transistor **112**. A source of the transistor **113** and a source of the transistor **112** are connected to the ground reference. A drain of the transistor **112** is connected to the input current terminal I_1. The operation of this circuit is well known to those skilled in the art, and does not need to be discussed in further detail here.

[0047] Referring to FIG. **2**, the gate signal terminal V_{GATE} drives the gate of the transistor **45**. Therefore, the current flowing from the source to the drain of the transistor **45** will be proportional to the current flowing from the source to the drain of the output pass transistor **10**. The physical dimensions of the output pass element **10** and the transistor **45** determine a proportion N, where the current flowing through the output pass transistor **10** will be N times the current flowing through the transistor **45**. In the

LDO voltage regulator according to the present invention, the proportion **N** is chosen such that the feedback current will not consume any more power than necessary in order to obtain an accurate high-frequency feedback signal. In many practical applications, typical values for **N** would be 500-1000.

[0048] The resistor **44** shown in FIG. **2** is required to have a large resistance (10 M Ω or more). In practice, however, it is very difficult to make a resistor with a large resistance in integrated circuits.

[0049] FIG. **5** demonstrates in detail how to build the resistor **44** with a large resistance. The resistor **44** includes a current sink **48** and two transistors **46** and **47**. A source of the transistor **46** is connected to the DC feedback terminal V_{FBDC}. A drain of the transistor **46** is connected to the positive input of the error amplifier **40**. A gate of the transistor **46** is connected to a gate of the transistor **47**, a drain of the transistor **47** and an input of the current sink **48**. A source of the transistor **47** is connected to the DC feedback terminal V_{FBDC}. An output of the current sink **48** is connected to the ground reference. The current sink **48** biases the transistor **46** to operate in linear mode, so that it acts as a resistor. The operation of current mirrors is well known to those skilled in the art, and does not need to be discussed in further detail here.

[0050] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims or their equivalents.